REMARKS

Claim Rejections - 35 U.S.C. § 102/103

The Examiner has rejected claims 1, 8, 9, and 12 under 35 U.S.C. § 102(b) as being anticipated by Krivokapic '587. The Examiner has rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9, and 12 above, and further in view of Takeuchi '351. The Examiner has rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9 and 12 above, and further in view of Choi '582. The Examiner has rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 in view of Takeuchi '351 as applied to claim 2 above, and further in view of Choi '582. The Examiner has rejected claims 5 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9 and 12 above, and further in view of Choi et al. '088. The Examiner has rejected claims 7, 10 and 11 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587. The Examiner has rejected claim 13 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 as applied to claims 1, 8, 9 and 12 above, and further in view of Pfiester '315 and further in view of Takeuchi '351. The Examiner has rejected claim 14 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 in view of Pfiester "315 in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi '582.

It is Applicant's understanding that the cited references fail to teach or render obvious Applicant's invention as claimed in claims 1-14. Applicant teaches and claims a MOS transistor having a gate electrode formed on a gate dielectric layer and a pair of source/drain regions. The source/drain regions are inwardly concaved

and create an inflection point 260, (Figure 2) beneath the gate electrode 202 and gate dielectric layer 204. That is, Applicant teaches and claims a MOS transistor structure which has source/drain regions which create an inflection point which are located beneath the gate dielectric layer 204 formed beneath the gate electrode 202.

It is Applicant's understanding that Krivokapic describes a transistor 300 (Figure 2p) which has a pair of source/drain regions 217 and 218. It is Applicant's understanding that the greatest laterally extending portion of the source and drain regions 217 and 218 do not extend beneath the gate electrode and gate dielectric layer as claimed by Applicant. Krivokapic, on the other hand, in Figure 2p shows a transistor having source/drain regions 217 and 218. A T-shaped gate electrode 210 is formed on a gate dielectric layer 208 (Figure 2j). Krivokapic includes a pair spacers 219 which are formed on pad oxide layer 202 (Figure 2j). The pad oxide layer 202 between the spacers 219 is then removed to expose a silicon substrate 201 (Figure 2i, Col. 6, lines 44-46). The gate oxide layer 208 is then formed on the substrate 201 between the spacers 219 where the pad oxide 202 was removed (Figure 2j). Krivokapic specifically states that "*the gate oxide 208 extends between the boundaries of the spacer 219 and the gate structure cavity 240 to replace pad oxide 202 that was previously removed*" (Col. 7, line 1-4). As shown in Figure 2p, the furthest laterally extending portions of the source and drain regions 217 and 218 extend beneath spacer 219 and pad oxide 202 and not beneath the gate electrode 210 and gate dielectric 208 as claimed by Applicant. As such, the combination of cited references clearly fail to teach or render obvious Applicant's invention as claimed in claims 1-14.

With respect to claims 13 and 14 Applicant teaches and claims a pair of silicon/germanium alloy source/drain regions formed in a substrate. Although Krivokapic describes a use of silicon source/drain regions, it is the Examiner's

position that it would have been obvious to of ordinary skill in the art to utilize silicon/germanium source/drain regions because Pfiester describes their use. It is Applicant's understanding that one of ordinary skill in the art would not be motivated to utilize Pfiester's silicon germanium source/drain regions in Krivokapic's transistor 300. It is to be appreciated that Krivokapic and Pfiester teach two totally different transistor structures and methods of fabrication. Krivokapic describes a standard transistor formed in a silicon substrate. Pfiester describes an elaborate thin film transistor having an inlaned thin film channel region. Krivokapic describes forming source/drain regions 217 and 218 utilizing ion-implantation and diffusion. Pfiester describes a process of depositing a silicon germanium film 20. An important aspect of Krivokapic is to form surfaces 224 in the silicon substrate 201 having a convex shape in order to obtain his desired source/drain profile. Applicant is unaware nor does the Examiner provide any suggestion on how one would integrate Pfiester's deposited silicon/germanium alloy film into Krivokapic's process to obtain silicon germanium alloy source/drain regions 217 and 218. The Examiner has used impermissible hindsight to pick and choose features among the cited references to reconstruct Applicant's claimed invention. As such, Applicant, therefore, respectfully requests the removal of the 35 U.S.C. § 103(a) rejections of claims 14 and 15 and seeks an early allowance of these claims.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 1/2/03

Michael A. Bernadicou
Reg. No. 35,934

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300